

Serial No.: 10/073,404
Filed: February 11, 2002

Group Art Unit: 2826
Examiner: V. Mandala

LISTING OF CLAIMS

Claim 1. (Currently amended) A power MOSFET device with reduced snap-back and being capable of increasing avalanche-breakdown current endurance, which has sequentially a drain with N⁺ silicon substrate, an N- epitaxial layer formed on said N⁺ silicon substrate, a source contact region formed of N⁺ doped well and P⁺ doped well implanted after etching in a P⁻ well formed on said N⁻ epitaxial layer, and a gate electrode with deposition of polysilicon above a channel region between said N⁻ epitaxial layer and N⁺ source contact region, said device is characterized in that: Said said source contact region is formed by etching into said P⁻ well first and implanting P⁺ dopant to the interface between said N⁻ epitaxial layer and P⁻ well, and the source contact region of said N⁺ well and that of said P⁺ well are not at the same level and are separated by at least a portion of the P⁻ well, by which it is possible to increase the avalanche-breakdown current durable capability of the power MOSFET device.

Claim 2. (Canceled)

Claim 3. (Currently amended) A power MOSFET device comprising:

an N⁺ silicon substrate;
a gate electrode;
an N⁻ epitaxial layer formed above said N⁺ silicon substrate, at least a portion of which is intermediate the N⁺ silicon substrate and the gate electrode;
a P⁻ well implanted in the N⁻ epitaxial layer;
a source contact region, etched into the P⁻ well, and formed of an N⁺ doped well and a P⁺ doped well, wherein the P⁺ doped well interfaces the N⁻ epitaxial layer and the P⁻ well, and the N⁺ doped well is located above the P⁺ doped well and separated from the P⁻ doped well by at least a portion of the P⁻ well spaced apart from and located above the P⁻ doped well; whereby the snap-back is reduced and the avalanche-breakdown current endurance is increased.

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Claims 4-8: (Cancelled)

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